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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,206	05/05/2004	Ian Chesal	015114-074300US	7267

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EXAMINER	
SIEK, VUTHE	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/840,206	CHESAL ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,12-17 and 19* is/are rejected.

7)☒ Claim(s) *9,11,18 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/840,206 filed on 5/5/2004. Claims 1-20 remain pending in the application.

Claim Objections

2. Claims 1 and 12 are objected to because of the following informalities: the limitation of "gathering **information** about the black box declarations and instances", **information** needed to be specified. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-6, 8, 12 and 14-17 rejected under 35 U.S.C. 102(e) as being anticipated by Levy (US 2004/0163072 A1).

5. As to claim 1 and 12, Levy teaches substantially the same claimed invention. Levy teaches a design automation system that allows entry of designs and converts the

design entities (black box and its instances that are art inherently) in HDL source file to register transfer level (RTL) hardware description language (HDL) (second and equivalent target design of new programmable logic integrated circuit compatible with HDL source code) (Fig. 2) (see summary). User input 31 (HDL source file of the designs including black box and its instances) is captured by a design entry system 32. Design entry system 32 allows the user to specify design entities (black box and its instances) for inclusion in a design, and includes a property acceptor 34 which functions to modify design entities selected using the design entry system 32. An HDL generator 36 automatically converts the design information gathered by the design entry system 32 into an RTL HDL target text file 38 suitable for use with simulators, hardware synthesis tools, integrated circuit layout tools, and other systems that accept RTL HDL input (0072). To facilitate automatic recognition of text that is to be processed by the system of the present invention, this embodiment uses a character sequence (Rx) included within the text (source file) (locating black block declarations and black box instances in the file). An HDL "use" statement 10 indicates a file named "Rx-package" which contains declarations of procedures and data types that are used in the conversion that allows a designer to express a design in a high-level, abstract language that is compatible with HDL (locating black box declarations and black box instances) (0081-0089). Fig. 3, 4a-b shows examples how to create equivalent black declarations and equivalent black box instances with the new programmable logic IC using information.

6. As to claims 3 and 14, Levy teaches automatically establishing interconnections of the design entities (0109).

7. As to claims 4 and 15, Levy teaches gathering information about the black box declaration comprising determining a number of input ports and output ports for each of the black box declarations (input/outputs configurations) (0109).

8. As to claims 5 and 16, Levy teaches gathering information about the black box instances comprising identifying input signals coupled to each input port of the black box instances, and identifying output signals coupled to each output port of the black box instances (0109, interconnections of the design entities).

9. As to claims 6 and 17, Levy teaches gathering information about the black box declarations comprising determining a function performed by each of the black box declarations (0092).

10. As to claim 8, Levy teaches stopping and restarting the codes that implement a design conversion process (translation process as shown in Fig. 2) for the circuit design without having to reparse the design conversion process from the beginning and saving a state of the design conversion to memory (0104-0106; Fig. 1-2).

11. Claims 1-6, 10, 12-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Sanders (6,536,017 B1).

12. As to claims 1 and 12, Sanders teaches a method for translating a first programmable logic device into a second and compatible programmable logic device with the first programmable logic device (Fig. 2-3). The circuit design (logic device A) is compatible with the circuit design (logic device B) because they are equivalent. The circuit design is written in source code file (HDL), where the circuit design (logic device A) is translated into compatible/equivalent circuit design (logic device B, second

programmable logic device). A report file of logic device A is generated (gathering information about a black box declarations and instances relating to the logic device A). A search process is performed to find compatible between the two logic devices. This would means finding compatible/equivalent of black box declarations and black box instances between the two logic devices A and B (see Fig. 2-3 description).

13. As to claims 2 and 13, Sanders teaches issuing a warning if incompatibility between the two logic devices are found or meaning that when an equivalent/compatible black box with new programmable logic IC cannot be located for one of the black box or declarations (col. 4 lines 52-67; col. 7 lines 28-40).

14. As to claims 3 and 14, Sanders teaches determining connections between signals to pins correspondences in the logic device (col. 5 lines 34-43)>

15. As to claims 4-6 and 15-17, Sanders teaches generating a report file that include number of input and output pins (ports) and connections there between; and a function performed by each of the black box declarations (col. 5 lines 45-64; col. 6 lines 26-65; col. 1, also see Fig. 2-3 description).

16. As to claims 10 and 19, Sanders teaches converting timing constraints associated with the circuit design to be compatible with the new programmable logic IC (second logic device) (Fig. 1-3; col. 5-6).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being obvious over Levy (US 2004/0163072 A1) in view of Leino et al. (7,024,661 2) or view of Sanders (6,536,017 B1).

19. As to claims 2 and 13, Levy does not teach a warning message. Leino et al. teach a warning message that is informative warning message and should be generated in order to show behavior of the design a given source location in order to make any necessary correction (col. 1). In addition, Sanders teaches issuing a warning as described in above rejection. With that motivation, it would have obvious to practitioners in the art at the time the invention was message to have include an informative warning message during the conversion process (translation) as taught by Levy when portions of source file 60 in Fig. 2 are not recognizable. This would mean that a warning message is generated if an equivalent black box compatible with the new programmable logic IC cannot be located for one of the black box instances or declarations.

20. Claim 7 is rejected under 35 U.S.C. 103(a) as being obvious over Levy (US 2004/0163072 A1) in view of Khakzaki et al. (US 2005/0114818 A1).

21. As to claim 7, Levy teaches written source code in HDL, but suggest other code can be used 0100). Khakzaki et al. teach using TCL scripts written in TCL code. The command processor uses a TCL command language interpreter to allow the user the capability to fully configure and change the contents of all menu, button and keyboard

accelerations at any time during run time. In addition, Khakzaki et al. teach each designer can use TCL scripts to create a custom environment, where the custom user environment can then be loaded on command and without logging off (0026-0033). With these motivations, it would have obvious to practitioners in the art at the time the invention was made to write source code in TCL code that is executed as a script sourced through an executable in a synthesis tool.

22. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Levy (US 2004/0163072 A1) in view of Sanders (6,536,017 B1).

23. As to claims 10 and 19, Levy does not teach timing constraints during conversion process. Sanders teach generating constraint file (timing constrains) during conversion process (col. 5 lines 45-67; col. 6 lines 1-26) in order to optimize the circuit design. With that motivation, it would have been obvious to practitioners in the art at the time the invention was made to converting timing constraints associated with the circuit design to be compatible with the new programmable logic IC.

Allowable Subject Matter

24. Claims 9, 11, 18 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach or fairly suggest generating a detailed report that indicates where the black box declarations and instances were found and the equivalent declarations and instances that the black box were replaced with; and identifying black box declarations in the file further comprising identifying blocks of code that do not have body definitions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER